CLAIMS

The invention claimed is:

1. A method of forming a circuit device, comprising:

forming a dielectric layer over a substrate;

forming a metal-containing material directly on the dielectric layer, the metal-containing material being formed to a thickness of no more than about 20Å; and

forming conductively-doped silicon directly on the metal-containing material.

2. The method of claim 1 wherein the conductively-doped silicon is majority n-type doped.

3. The method of claim 1 wherein the conductively-doped silicon is n-type doped, and wherein a work function of the conductively-doped silicon and metal-containing material together is shifted relative to the work functions of the conductively-doped silicon and the metal-containing material in pure form, and is shifted from the work function of the metal-containing material in pure form by at least 50 millivolts.

4. The method of claim 1 wherein:

the circuit device is a capacitor construction,

the substrate comprises a first electrical node of the capacitor, and

the conductively-doped silicon is comprised by a second electrical node spaced from the first electrical node by at least the dielectric material.

5. The method of claim 1 wherein:

the circuit device is a transistor,

the dielectric is comprised by a gate dielectric, and

the conductively-doped silicon is comprised by a gate.

6. The method of claim 1 wherein forming the conductively-doped silicon comprises deposition of silicon on the metal-containing material, and wherein a composition comprising silicon and metal of the metal-containing material forms at the interface of the metal-containing material and the silicon.

7. The method of claim 1 wherein the dielectric layer comprises a high k dielectric material.

8. The method of claim 1 wherein the dielectric layer comprises one or more of tantalum, hafnium and aluminum.

9. The method of claim 1 wherein the metal-containing material comprises one or more of titanium nitride, tantalum nitride, hafnium nitride and tungsten nitride.

10. The method of claim 1 wherein the metal-containing material comprises one or more of titanium silicide, tantalum silicide, hafnium silicide and tungsten silicide.

11. The method of claim 1 wherein the metal of the metal-containing material comprises one or more of titanium, tungsten, hafnium and tantalum.

12. The method of claim 1 wherein the metal of the metal-containing material consists essentially of one or more of titanium, tungsten, hafnium and tantalum.

13. The method of claim 1 wherein the metal of the metal-containing material consists of one or more of titanium, tungsten, hafnium and tantalum.

14. The method of claim 1 wherein the thickness of the metal-containing material is less than or equal to about 15Å.

15. The method of claim 1 wherein the thickness of the metal-containing material is less than or equal to about 10Å.

16. A method of forming a transistor device, comprising:

forming a gate dielectric layer over a substrate;

forming a metal-containing material over the dielectric layer, the metal-containing material being formed with no more than about 70 ALD cycles;

forming conductively-doped silicon over the metal-containing material;

patterning the metal-containing material and conductively-doped silicon into a gate stack; and

providing source/drain regions proximate the gate stack.

17. The method of claim 16 wherein the conductively-doped silicon is majority n-type doped.

18. The method of claim 16 wherein the conductively-doped silicon is n-type doped, and wherein a work function of the conductively-doped silicon and metal-containing material together is shifted relative to the work functions of the conductively-doped silicon and the metal-containing material in pure form, and is shifted from the work function of the metal-containing material in pure form by at least 50 millivolts.

19. The method of claim 16 wherein forming the conductively-doped silicon comprises deposition of silicon on the metal-containing material, and wherein a composition comprising silicon and metal of the metal-containing material forms at the interface of the metal-containing material and the silicon.

20. The method of claim 16 wherein the dielectric layer comprises a high k dielectric material.

21. The method of claim 16 wherein the dielectric layer comprises one or more of tantalum, hafnium and aluminum.

22. The method of claim 16 wherein the metal-containing material comprises one or more of titanium nitride, tantalum nitride, hafnium nitride and tungsten nitride.

23. The method of claim 16 wherein the metal-containing material comprises one or more of titanium silicide, tantalum silicide, hafnium silicide and tungsten silicide.

24. The method of claim 16 wherein the metal of the metal-containing material predominately comprises titanium.

25. The method of claim 16 wherein the metal of the metal-containing material predominately comprises tantalum.

26. The method of claim 16 wherein the metal of the metal-containing material predominately comprises hafnium.

27. The method of claim 16 wherein the metal of the metal-containing material predominately comprises tungsten.

28. The method of claim 16 wherein the metal-containing material has a thickness of less than or equal to about 20Å.

29. The method of claim 16 wherein the metal-containing material has a thickness of less than or equal to about 15Å.

30. The method of claim 16 wherein the metal-containing material has a thickness of less than or equal to about 10Å.

31. A method of forming a PMOS device and an NMOS device, comprising:

providing substrate comprising a PMOS gate region and an NMOS gate region;

forming a gate dielectric layer over the PMOS and NMOS gate regions of the substrate;

forming a thick metal-containing material to be over the PMOS gate region and not over the NMOS gate region, the thick metal-containing material being formed to a thickness of greater than 20Å;

forming a thin metal-containing material to be over the PMOS and NMOS gate regions, the thin metal-containing material being formed to a thickness of less than or equal to about 20Å and being formed over the thick metal-containing material over the PMOS gate region;

forming a layer of conductively-doped silicon extending across the PMOS and NMOS gate regions and over the thin metal-containing material;

incorporating the thick metal-containing material, thin metal-containing material and conductively-doped silicon into a PMOS transistor gate stack over the PMOS gate region; and

incorporating the thin metal-containing material and conductively-doped silicon into an NMOS transistor gate stack over the NMOS gate region.

32. The method of claim 31 wherein the conductively-doped silicon is majority n-type doped.

33. The method of claim 31 wherein the gate dielectric layer comprises one or more of tantalum, hafnium and aluminum.

34. The method of claim 31 wherein the gate dielectric layer comprises aluminum oxide over silicon dioxide.

35. The method of claim 31 wherein the thin metal-containing material comprises one or more of titanium nitride, tantalum nitride, hafnium nitride and tungsten nitride.

36. The method of claim 31 wherein the thin metal-containing material comprises one or more of titanium silicide, tantalum silicide, hafnium silicide and tungsten silicide.

37. The method of claim 31 wherein the metal of the thin metal-containing material predominately comprises one or more of titanium, tantalum, tungsten and hafnium.

38. The method of claim 31 wherein the thickness of the thin metal-containing material is less than or equal to about 15Å.

39. The method of claim 31 wherein the thickness of the thin metal-containing material is than or equal to about 10Å.

40. A method of forming a capacitor construction, comprising:

forming a dielectric layer over a capacitor storage node;

forming a metal-containing material over the dielectric layer, the metal-containing material being formed with less than or equal to about 70 ALD cycles; and

forming conductively-doped silicon over the metal-containing material.

41. The method of claim 40 wherein the conductively-doped silicon is majority n-type doped.

42. The method of claim 40 wherein the dielectric layer comprises one or more of tantalum, hafnium and aluminum.

43. The method of claim 40 wherein the metal-containing material comprises one or more of titanium nitride, tantalum nitride, hafnium nitride and tungsten nitride.

44. The method of claim 40 wherein the metal-containing material comprises one or more of titanium silicide, tantalum silicide, hafnium silicide and tungsten silicide.

45. The method of claim 40 wherein the metal of the metal-containing material predominately comprises one or more of titanium, tantalum, hafnium and tungsten.

46. The method of claim 40 wherein the metal-containing material has a thickness of less than or equal to about 20Å.

47. The method of claim 40 wherein the metal-containing material has a thickness of less than or equal to about 15Å.

48. The method of claim 40 wherein the metal-containing material has a thickness of less than or equal to about 10Å.

49. A method of forming a capacitor construction, comprising:

forming a capacitor electrode comprising conductively-doped silicon; and

providing a metal-containing material between the capacitor electrode and a capacitor dielectric layer, the metal-containing material having a thickness of no more than about 20Å.

50. The method of claim 49 wherein the conductively-doped silicon is majority n-type doped.

51. The method of claim 49 wherein the dielectric layer comprises one or more of tantalum, hafnium and aluminum.

52. The method of claim 49 wherein the dielectric layer comprises aluminum oxide.

53. The method of claim 49 wherein the metal of the metal-containing material predominately comprises one or more of titanium, tantalum, hafnium and tungsten.

54. The method of claim 49 wherein the metal-containing material comprises one or more of titanium nitride, tantalum nitride, hafnium nitride and tungsten nitride.

55. The method of claim 49 wherein the metal-containing material comprises one or more of titanium silicide, tantalum silicide, hafnium silicide and tungsten silicide.

56. The method of claim 49 wherein the thickness of the metal-containing material is less than or equal to about 15Å.

57. The method of claim 49 wherein the thickness of the metal-containing material is less than or equal to about 10Å.

58. A transistor device, comprising:

a gate dielectric layer over a substrate;

a gate stack over the gate dielectric layer, and

source/drain regions proximate the gate stack; and wherein the gate stack comprises:

a metal-containing material over the dielectric layer, the metal-containing material having a thickness of no more than about 20Å; and

a conductively-doped silicon layer over the metal-containing material.

59. The transistor device of claim 58 wherein the conductively-doped silicon is majority n-type doped.

60. The transistor device of claim 58 wherein the dielectric layer comprises one or more of tantalum, hafnium and aluminum.

61. The transistor device of claim 58 wherein the dielectric layer comprises aluminum oxide.

62. The transistor device of claim 61 wherein the metal-containing material is physically against the aluminum oxide.

63. The transistor device of claim 61 wherein the dielectric layer comprises the aluminum oxide over silicon dioxide.

64. The transistor device of claim 58 wherein the metal of the metal-containing material predominately comprises one or more of titanium, tungsten, tantalum and hafnium.

65. The transistor device of claim 58 wherein the metal-containing material predominately comprises one or more of titanium nitride, tungsten nitride, tantalum nitride and hafnium nitride.

66. The transistor device of claim 58 wherein the thickness of the metal-containing material is less than or equal to about 15Å.

67. The transistor device of claim 58 wherein the thickness of the metal-containing material is less than or equal to about 10Å.

68. An electronic system comprising the transistor device of claim 58.

69. A CMOS, comprising:

a dielectric layer over a substrate;

a PMOS gate and an NMOS gate over the dielectric layer;

a first metal-containing material within the PMOS gate and over the dielectric layer, the first metal-containing material having a thickness of greater than 20Å;

a second metal-containing material within the NMOS gate and over the dielectric layer, the second metal-containing material having a thickness of less than or equal to about 20Å;

a first layer of n-type doped silicon within the PMOS gate and over the first metal-containing material; and

a second layer of n-type doped silicon within the NMOS gate and over the second metal-containing material.

70. The CMOS of claim 69 wherein the dielectric layer comprises one or more of tantalum, hafnium and aluminum.

71. The CMOS of claim 69 wherein the dielectric layer comprises aluminum oxide.

72. The CMOS of claim 71 wherein the first and second metal-containing materials are physically against the aluminum oxide.

73. The CMOS of claim 69 wherein the first and second metal-containing materials have the same composition as one another.

74. The CMOS of claim 73 wherein the first and second metal-containing materials predominately comprise one or more of titanium nitride, tantalum nitride, tungsten nitride and hafnium nitride.

75. The CMOS of claim 73 wherein the first and second metal-containing materials predominately comprise one or more of titanium silicide, tantalum silicide, tungsten silicide and hafnium silicide.

76. The CMOS of claim 69 wherein the thickness of the second metal-containing material is less than or equal to about 15Å.

77. The CMOS of claim 69 wherein the thickness of the second metal-containing material is less than or equal to about 10Å.

78. The CMOS of claim 69 wherein the thickness of the first metal-containing material is greater than or equal to about 100Å.

79. The CMOS of claim 69 wherein the thickness of the first metal-containing material is greater than or equal to about 150Å.

80. The CMOS of claim 69 wherein the thickness of the first metal-containing material is greater than or equal to about 150Å, and wherein the thickness of the second metal-containing material is less than or equal to about 15Å.

81. An electronic system comprising the CMOS of claim 69.

82. A capacitor construction, comprising:

a first capacitor electrode, the first capacitor electrode comprising conductively-doped silicon;

a dielectric layer proximate the first capacitor electrode;

a second capacitor electrode across the dielectric layer from the first capacitor electrode; and

a metal-containing material between the conductively-doped silicon of the first capacitor electrode and the dielectric layer, the metal-containing material having a thickness of less than or equal to about 20Å.

83. The capacitor construction of claim 82 wherein the second capacitor electrode is a storage node of the capacitor.

84. The capacitor construction of claim 83 wherein the second capacitor electrode comprises rugged silicon.

85. The capacitor construction of claim 82 wherein the conductively-doped silicon is majority n-type doped.

86. The capacitor construction of claim 82 wherein the dielectric layer comprises one or more of tantalum, hafnium and aluminum.

87. The capacitor construction of claim 82 wherein the dielectric layer comprises aluminum oxide.

88. The capacitor construction of claim 87 wherein the metal-containing material is physically against the aluminum oxide.

89. The capacitor construction of claim 82 wherein the metal-containing material predominately comprises one or more of titanium nitride, tantalum nitride, tungsten nitride and hafnium nitride.

90. The capacitor construction of claim 82 wherein the metal-containing material predominately comprises one or more of titanium silicide, tantalum silicide, tungsten silicide and hafnium silicide.

91. The capacitor construction of claim 82 wherein the thickness of the metal-containing material is less than or equal to about 15Å.

92. The capacitor construction of claim 82 wherein the thickness of the metal-containing material is less than or equal to about 10Å.

93. A DRAM comprising the capacitor construction of claim 82.

94. An electronic system comprising the DRAM of claim 93.